NSF 24-522

NSF – Enabling Access to the Semiconductor Chip Ecosystem for Design, Fabrication, and Training

(Chip Design Hub)

January 22, 2024

NSF Chip Design Hub Program – Webinar

Use the Q&A panel in Zoom to send questions—we'll answer some at the end

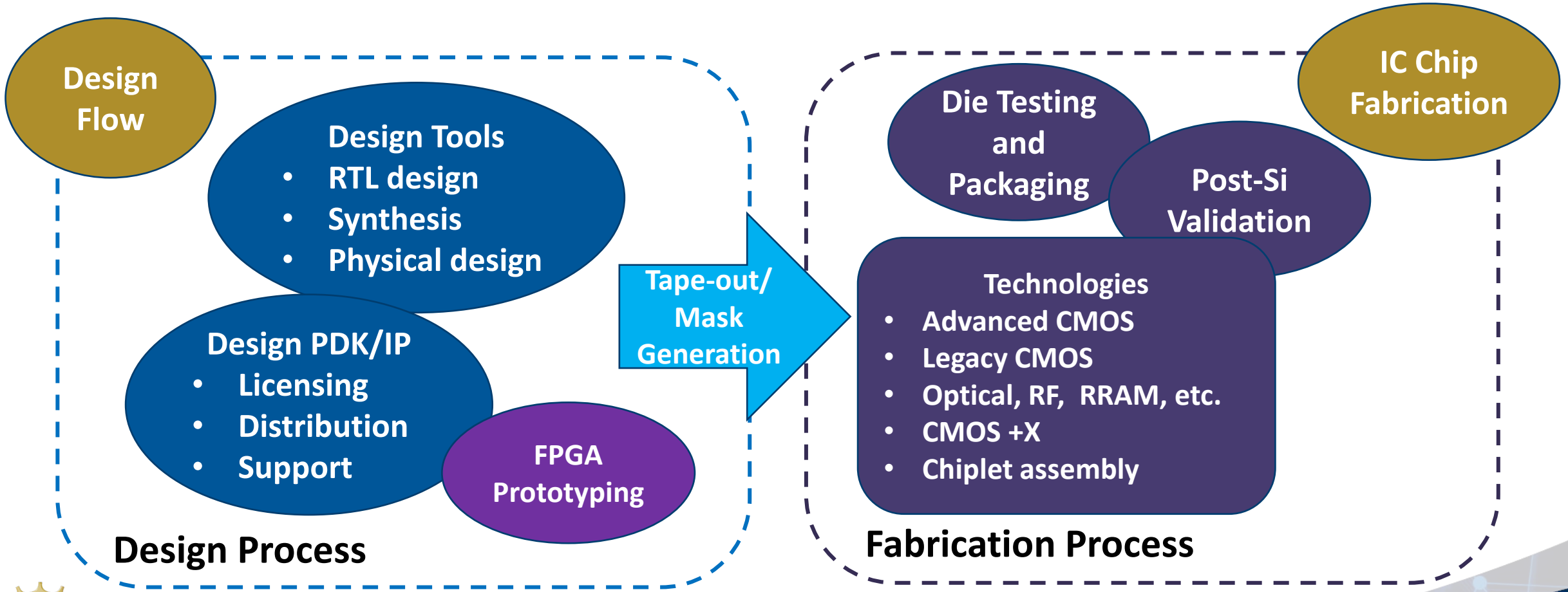
After the webinar, send questions to chip_hub@nsf.gov

Live transcript is available through Zoom

Solicitation page:

https://new.nsf.gov/funding/opportunities/enabling-access-semiconductor-chip-ecosystem

IC Chip Design and Fabrication Infrastructure: Key Components



Voices from the Community: What NSF Should Do

- **NSF Workshop on Micro/Nano Circuits and Systems Design and Design Automation (December 2020)**

  https://nsfedaworkshop.nd.edu/

- **Foundry Meeting co-located with the above workshop (December 2020)**

  https://nsfedaworkshop.nd.edu/foundry-meeting/

- **NSF Integrated Circuit Research, Education and Workforce Development Workshop (October 2021/May 2022)**

  https://nsf-ic-education.com/

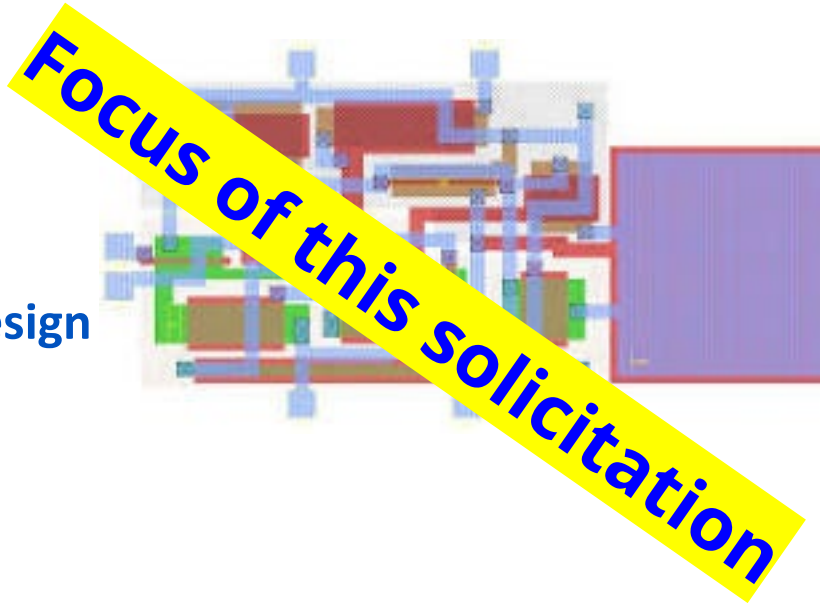
- **NSF CHIPS Education and Workforce Development Convening (November 2023)**

  https://micronanoeducation.org/sewc/

- **CISE RFI on Semiconductor Research and Education**

  https://www.nsf.gov/cise/semiconductors/RFISummary-Report.pdf

Key Takeaways: Design Infrastructure



- Open access for IC design ecosystem
  - EDA tool license/access and maintenance, IP cores, etc.
  - Training materials at *all levels* for both FPGA prototype and IC design
- Design enablement for emerging technologies
  - Design and verification tools to address emerging technologies
  - System-level demonstrations of emerging technologies
- Partner with software vendors to fund licenses especially for k-14 institutions

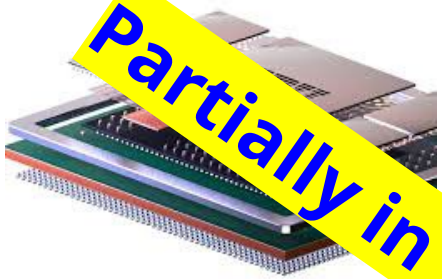
=> Make the IC design process as easy as software development

Key Takeaways: Fabrication Infrastructure

- Access to leading-edge and legacy silicon CMOS technologies
  - Support the cost of chip tape out
- Establish a national facility for prototyping emerging technologies at-scale
  - Beyond the 1 to 1,000 devices scale
  - Integration of various materials and devices on the Si CMOS foundry wafer
  - Fast turn-around experimentation of chip-scale, and package-scale systems
- Tape-out and fabrication should be supported at no or very low cost to students
  - Different type of support for different level of students

Key Takeaways: Packaging and Testing Infrastructure

- Establish and coordinate regional/national facilities for remote chip testing
  - Cloud access
  - Sharing equipment and expertise
  - Sharable test boards



Partially in this solicitation

- Establish nationally accessible multi-project packaging service
  - Chiplet/interposer/PCB offerings and associated assembly design kits
  - Access to heterogenous, chiplet integration

Enabling Access to the Semiconductor Chip Ecosystem for Design, Fabrication, and Training (Chip Design Hub)

PROGRAM SOLICITATION

NSF 24-522

National Science Foundation

Directorate for Computer and Information Science and Engineering

Division of Computing and Communication Foundations

Division of Computer and Network Systems

Full Proposal Deadline(s) (due by 5 p.m. submitter's local time):

April 04, 2024

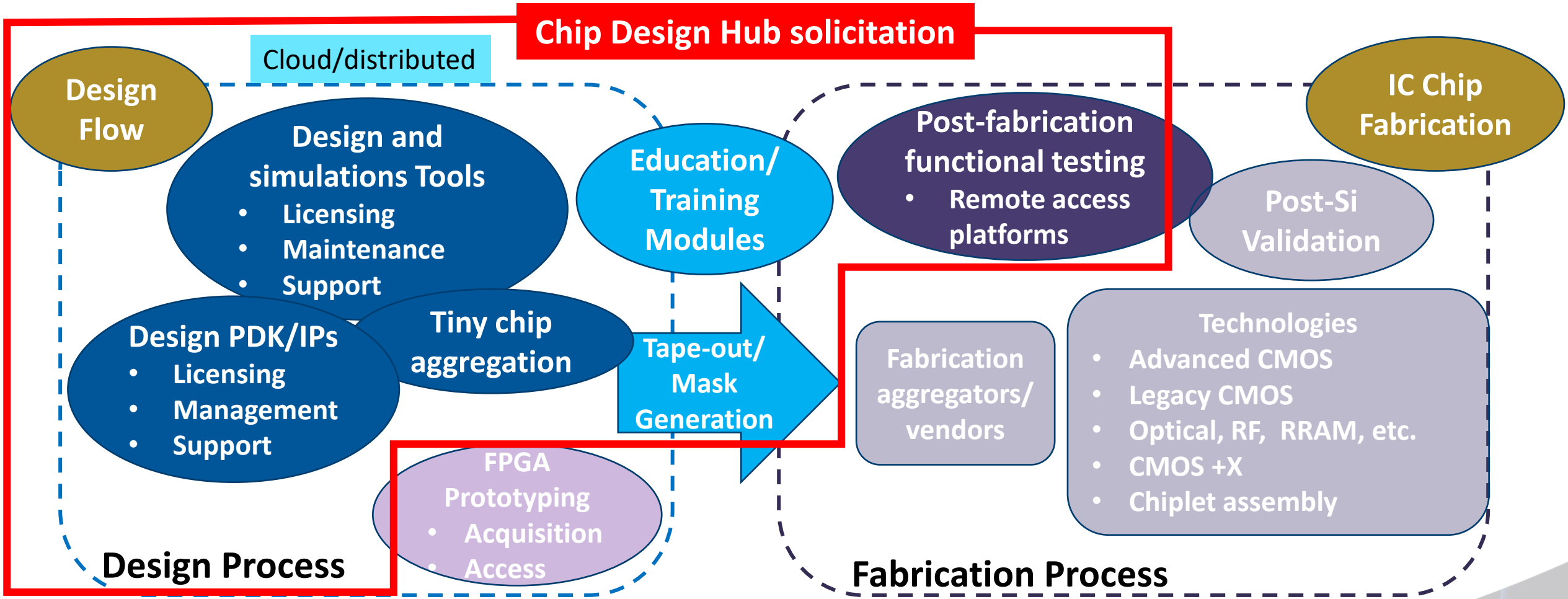
Overarching Objectives of the Chip Design Hub Solicitation

- Dramatically lower the barriers for students to access
  - State-of-the-art electronic design automation (EDA) tools
  - Process design kits (PDKs), and
  - Design intellectual property (IP) cores

- Enable students at various levels to design and test IC chips

A key goal is to broaden participation in IC chip design beyond the small number of institutions currently engaged in these activities

IC Chip Design and Fabrication Infrastructure: Key Components



Both commercial tools and and open-source tools

Foundries, fabrication brokers, academic facilities

Chip Design Hub

Providing cloud-based design enablement to IHEs and beyond

- EDA Tools
  - Access to end-to-end tool flows, with licenses and version requirements
    - Inclusion of EDA tools from both multiple vendors and open-source tools is highly desirable
    - The tool suite should include both front-end and back-end design and verification tools
- Process Design Kits (PDKs) and IP (Intellectual Property)
  - Access to a variety of PDKs and IP resources
    - either hard or soft cores depending on the requirements
- Education and training
  - Include comprehensive educational material for chip design, verification, yield analysis, etc.
  - Provide in-depth training on best practices towards a successful tape-out

Chip Design Hub

Providing cloud-based design enablement to IHEs and beyond

- IC chip designs from the design flow: Mask layout files suitable for fabrication
- Main focus on access to tools and IP/PDKs for fabrication on standard CMOS processes
  - Emerging technologies and predictive PDKs and design kits are welcome
- Post-fabrication supports such as packaging, board design, testing, etc., are welcome
  - E.g., In the form of tools, design guidelines, training materials, etc.
  - Providing remote access to reduce the overall cost born by students and researchers is desirable
- **This program will not support projects that include science and engineering research (except for validating the readiness of the proposed infrastructure)**

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April 04, 2024

- **Letters of Intent: Not required**
- **Preliminary Proposal Submission: Not required**
- **Proposal Deadline: April 4, 2024, 5PM local time**
- **Full Proposals submitted via research.gov or grants.gov**

Chip Design Hub Award Information

Anticipated Type of award: Cooperative Agreement

Estimated Number of Awards: 2

Anticipated Funding Amount: $10,000,000

The maximum size and duration of an award will be up to $1.6 million per year for up to 5 years.

Estimated program budget, number of awards and average award size/duration are subject to the availability of funds

Eligibility Information

- PI and co-PI(s) must hold either:
  - a tenured or tenure-track position, or
  - a primary, full-time, paid appointment in a research or teaching position
- Individuals at overseas branch campuses of US IHEs are not eligible
- Individuals with primary appointments at for-profit non-academic organizations can serve as paid or unpaid Senior Personnel (i.e., not as PIs nor co-PIs)
- An individual may appear as PI, co-PI, senior personnel on only ONE proposal
- No limit on the number of proposals per organization
- A single (not collaborative) proposal should be submitted by the lead organization
  - Support provided to collaborating organizations via subawards

Proposal Preparation Instructions

- **Refer to PAPPG Chapter II.D.2 for guidance on the required sections**

- Pay attention to the instructions that deviate from the PAPPG instructions
- **Additional supplementary documentation**
  - **Collaboration Plan: required, up to 2 pages, including:**
    - Specific roles of all participants involved
    - How the project will be managed across all the participants and institutions
    - Coordination mechanisms for cross-investigator, cross-institution, and/or cross-discipline integration
  - **Letter of Collaboration: required, if involving industry partners**
    - Plan for interaction, the time commitment of the industrial partner(s), and the nature of the work
    - # of identified (unfunded) collaborators <= 10

Multi-University Collaboration and Industry Engagement

- Highly encouraged

- Industry partners may include but not limited to
  - EDA companies
  - foundry brokers
  - foundries

- Other types of non-profit and for-profit organizations (not IHEs) can also be collaborators

- Roles and activities should be clearly described

- Refer to the previous pages regarding eligibility criteria and collaboration plan

Solicitation Specific Merit Review Criteria
(see solicitation for details)

- Enabling new research directions
  - that were previously intractable, infeasible, or impractical prior to this project
- Addressing education and workforce development addressed
  - Strengthen post-secondary education
  - Have measurably positive impact on the semiconductor workforce
- The range of semiconductor-based systems enabled
  - CMOS fabrication at different feature sizes, other technologies
- Plans for engaging the user community
  - Validating the impact of the project investment
  - Sustainability beyond the initial NSF investment
- Plans for engaging with open-source, academic, and non-academic entities

Additional Considerations: Cybersecurity Plan

- Describe roles and responsibilities w.r.t. cybersecurity for the facility
  - Technical safeguards
  - Administrative safeguards
  - Physical safeguards
  - Policies and procedures for cybersecurity
  - Plans for awareness and training
  - Procedures for notification to NSF, the IC design community, other relevant communities, and appropriate authorities (e.g., local police, the Federal Bureau of Investigation)
- Also describe
  - How the effectiveness of the proposed cybersecurity program will be evaluated and assessed
  - What approach will be taken to implement the cybersecurity plan

Review Process and Special Award Conditions

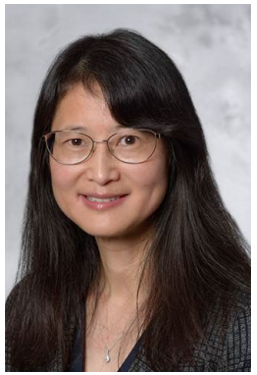
- Proposals will be reviewed by Ad hoc Review and/or Panel Review, plus (Reverse) Site Visit Review
- Awards will be made in the form of cooperative agreements
- Within the first 90 days of the award, a retreat, organized by the award recipient, will be required
  - The budget should include expenses for this retreat
- NSF may conduct site visits and/or reverse site visits as part of the proposal evaluation process and subsequent review of the project performance
- Support for each year of a funded project will be contingent upon a satisfactory annual review
- All funding is subject to availability

Program Directors Managing NSF 24-522

CISE/CCF


Sankar Basu


X. Sharon Hu


Danella Zhao

CISE/CNS


Erik Brunvand


Daniel Andressen


Jason Hallstrom

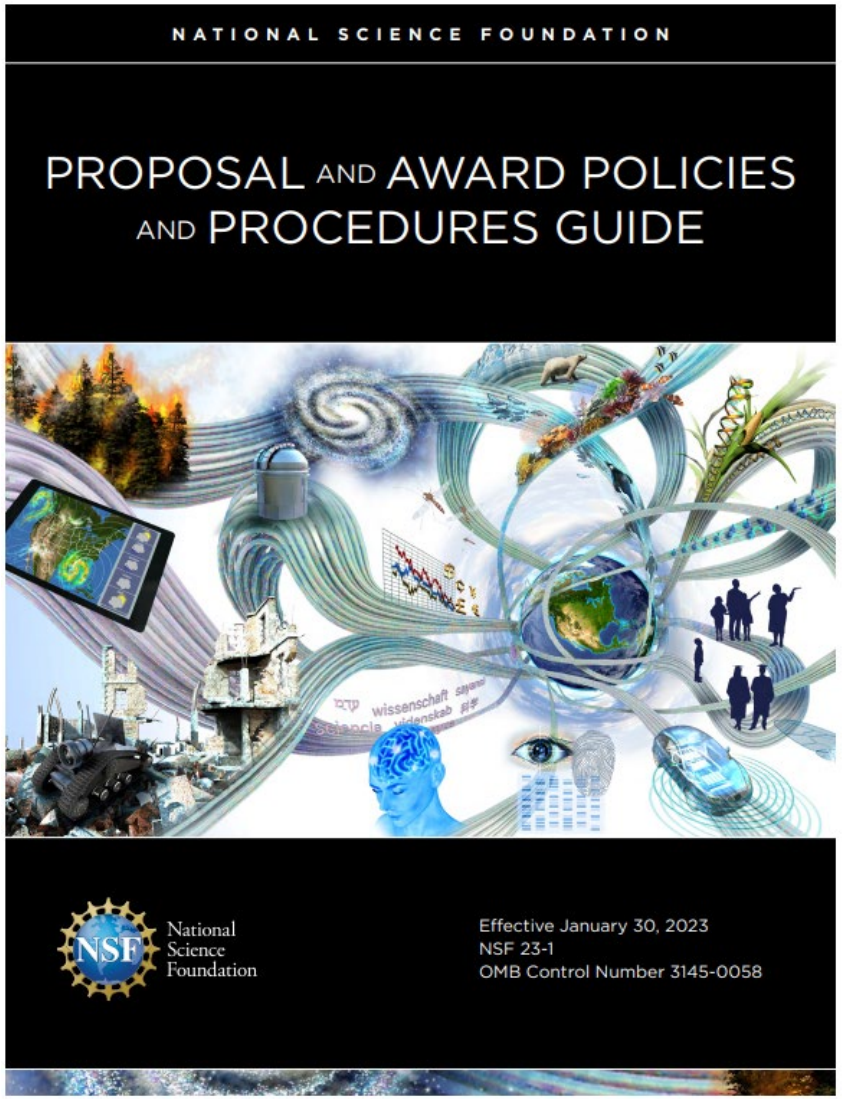
IIS


Raj Acharya

OAC


Andrey Kanaev

General and specific inquiries regarding this funding opportunity should be sent to email: chip_hub@nsf.gov



Resources and Program Officers are Available to Help

- Be sure to fully read the solicitation NSF 24-522
- Be sure to fully read the PAPPG
  - PAPPG Part 1-Chapter 2 – Proposal preparation guide
  - PAPPG Exhibit II-1
  - Proposal Checklist
- Email: chip_hub@nsf.gov

Q&A

- **Please use the Q&A panel in Zoom to submit questions**
- **After the webinar, email your questions to chip_hub@nsf.gov**
- **Check Webinar Materials and updated Chip Desigb Hub FAQ online**

https://new.nsf.gov/events/chip-design-hub-program-webinar

THANK YOU